IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:
Perez, et al. Atty. Docket No.: BUR920030032US1

Serial No.: 10/604,059 Group Art Unit: 2825

Filed: June 24, 2003 Examiner: Doan, Nghia M.

For: METHOD OF DISPLAYING A GUARD RING WITHIN AN INTEGRATED CIRCUIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' APPEAL BRIEF

Sirs:

Appellants respectfully appeal the final rejection of claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44, in the Office Action dated March 21, 2007. A Notice of Appeal and Pre-Appeal Brief Request for Review were timely filed on May 17, 2007.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, Armonk, New York, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44, all the claims pending in the application, stand rejected under 35 U.S.C. §102(b) as being anticipated by Ker, et al. ("Automatic Methodology for Placing the Guard Rings into Chip Layout to Prevent Latchup in CMOS IC's," IEEE, Vol. 1, September 2001, pp. 113-116), hereinafter "Ker."

IV. STATUS OF AMENDMENTS

In response to an Office Action mailed on March 21, 2007 (hereinafter referred to as "the Office Action"), an after-final Response that made no claim amendments was filed on April 19, 2007. An Advisory Action dated April 25, 2007 indicated that, upon filing an appeal, the Response filed on April 19, 2007 did not place the application in

condition for allowance, and that the rejections of claims would remain. The claims shown in the appendix are shown in their amended form as of the March 14, 2007 Supplemental Amendment.

V. SUMMARY OF CLAIMED SUBJECT MATTER

One feature of the invention is displaying a guard ring within an integrated circuit design having logic devices. Claim 1 defines this feature as follows: "displaying a guard ring within an integrated circuit design having logic devices." This feature is described at various points in the specification, for example paragraph [0045] describes this feature as follows: "the circuit-type of indication unit 20 to classify the circuit to which the guard ring is being added ". This is shown in Figure 2.

Another feature of the invention is determining positions of the logic devices within the integrated circuit design. Claim 1 defines this feature as follows: "determining positions of said logic devices within said integrated circuit design." This feature is described at various points in the specification, for example paragraph [0045] describes this feature as follows: "From the identification of the circuit type, the invention can automatically determine the types of guard rings which are appropriate for a given circuit which allows the guard ring to be auto-generated or manually created using graphical user interface (GUI)". This is shown in Figure 2.

Another feature of the invention is incorporating the guard ring into the integrated circuit design. Claim 1 defines this feature as follows: "incorporating said guard ring into said integrated circuit design." This feature is described at various points in the

specification, for example paragraph [0045] describes this feature as follows: "uses the circuit-type of indication unit 20 to classify the circuit to which the guard ring is being added ". This is shown in Figure 2.

Another feature of the invention is displaying the logic devices and the guard ring symbolically and schematically in a single integrated display. Claim 1 defines this feature as follows: "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display." This feature is described at various points in the specification, for example paragraph [0056] describes this feature as follows: "the guard ring P-cell 131 and hierarchical ESD P-cell 132 are combined to form the ESD guard ring hierarchical design 130". This is shown in Figure 13.

Another feature of the invention is the displaying of the logic devices and the guard ring symbolically comprises displaying a parameterized symbol. Claim 1 defines this feature as follows: "wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol." This feature is described at various points in the specification, for example paragraph [0043] describes this feature as follows: "a design system structure of the present invention that integrates a parameterized cell (P-cell) design 10 and definition 13 using graphical 11 and schematic 12 representations ". This is shown in Figure 1.

Another feature of the invention is the parameterized symbol comprises parameters. Claim 1 defines this feature as follows: "wherein said parameterized symbol comprises parameters." This feature is described at various points in the specification, for example paragraph [0053] describes this feature as follows: "parameterized cell

contains both graphical and circuit representation, as well as a symbol function". This is shown in Figure 10.

Another feature of the invention is the parameters comprise at least one of a type of the guard ring and an efficiency of the guard ring. Claim 1 defines this feature as follows: "wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring." This feature is described at various points in the specification, for example paragraph [0053] describes this feature as follows: "By integrating a guard ring P-cell 100 with the ESD P-cell, parasitic devices, the guard ring efficiency, and latchup robustness can be evaluated". This is shown in Figure 10.

Another feature of the invention is displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and the at least one guard ring. Claim 13 defines this feature as follows: "displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and said at least one guard ring." This feature is described at various points in the specification, for example paragraph [0051] describes this feature as follows: "the new P-cell is modified in that it is now contain all the data information of the parameterized cell guard ring as well as the ESD P-cell ". This is shown in Figure 8.

Another feature of the invention is establishing positions of the logic devices within a portion of the hierarchical integrated circuit design. Claim 13 defines this feature as follows: "establishing positions of said logic devices within a portion of said hierarchical integrated circuit design." This feature is described at various points in the specification, for example paragraph [0046] describes this feature as follows: "By

evaluation of the circuit hierarchy, the circuit type and class can be identified". This is shown in Figure 3.

Another feature of the invention is incorporating the guard ring into the portion of the hierarchical integrated circuit design. Claim 13 defines this feature as follows: "incorporating said guard ring into said portion of said hierarchical integrated circuit design." This feature is described at various points in the specification, for example paragraph [0048] describes this feature as follows: "The combined guard ring and P-cell are produced and can be used in a hierarchical circuit design 53". This is shown in Figure 5.

Another feature of the invention is displaying the portion of the integrated circuit design as a cell having the guard ring within the hierarchical integrated circuit design. Claim 13 defines this feature as follows: "displaying said portion of said integrated circuit design as a cell having said guard ring within said hierarchical integrated circuit design." This feature is described at various points in the specification, for example paragraph [0051] describes this feature as follows: "Figure 7 is a graphical illustration of an input node ESD P-cell that can be used in a hierarchical design. This P-cell includes voltage lines VDD 70 and VSS 72 P+/N- well diodes 71 that are positioned between the stretch lines 73. This P-cell can be auto-generated and actually contains two primitive parameterized (twin diodes). Figure 8 illustrates the same structure as that shown in Figure 7 and includes the guard ring 80. In this implementation, the new P-cell is modified in that it is now contain all the data information of the parameterized cell guard ring as well as the ESD P-cell". This is shown in Figure 8.

Another feature of the invention is the displaying of the portion of the integrated circuit design comprises displaying the logic devices and the guard ring symbolically and schematically in a single integrated display. Claim 13 defines this feature as follows: "wherein said displaying of said portion of said integrated circuit design comprises displaying said logic devices and said guard ring symbolically and schematically in a single integrated display." This feature is described at various points in the specification, for example paragraph [0056] describes this feature as follows: "the guard ring P-cell 131 and hierarchical ESD P-cell 132 are combined to form the ESD guard ring hierarchical design 130". This is shown in Figure 13.

Another feature of the invention is the displaying of the logic devices and the guard ring symbolically comprises displaying a parameterized symbol. Claim 13 defines this feature as follows: "wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol." This feature is described at various points in the specification, for example paragraph [0043] describes this feature as follows: "a design system structure of the present invention that integrates a parameterized cell (P-cell) design 10 and definition 13 using graphical 11 and schematic 12 representations ". This is shown in Figure 1.

Another feature of the invention is the parameterized symbol comprises parameters. Claim 13 defines this feature as follows: "wherein said parameterized symbol comprises parameters." This feature is described at various points in the specification, for example paragraph [0053] describes this feature as follows:

"parameterized cell contains both graphical and circuit representation, as well as a symbol function". This is shown in Figure 10.

Another feature of the invention is the parameters comprise at least one of a type of the guard ring and an efficiency of the guard ring. Claim 13 defines this feature as follows: "wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring." This feature is described at various points in the specification, for example paragraph [0053] describes this feature as follows: "By integrating a guard ring P-cell 100 with the ESD P-cell, parasitic devices, the guard ring efficiency, and latchup robustness can be evaluated". This is shown in Figure 10.

Another feature of the invention is displaying a guard ring within an integrated circuit design having logic devices. Claim 25 defines this feature as follows: "displaying a guard ring within an integrated circuit design having logic devices." This feature is described at various points in the specification, for example paragraph [0045] describes this feature as follows: "the circuit-type of indication unit 20 to classify the circuit to which the guard ring is being added ". This is shown in Figure 2.

Another feature of the invention is determining positions of the logic devices within the integrated circuit design. Claim 25 defines this feature as follows: "determining positions of said logic devices within said integrated circuit design." This feature is described at various points in the specification, for example paragraph [0045] describes this feature as follows: "From the identification of the circuit type, the invention can automatically determine the types of guard rings which are appropriate for

a given circuit which allows the guard ring to be auto-generated or manually created using graphical user interface (GUI)". This is shown in Figure 2.

Another feature of the invention is incorporating the guard ring into the integrated circuit design. Claim 25 defines this feature as follows: "incorporating said guard ring into said integrated circuit design." This feature is described at various points in the specification, for example paragraph [0045] describes this feature as follows: "uses the circuit-type of indication unit 20 to classify the circuit to which the guard ring is being added ". This is shown in Figure 2.

Another feature of the invention is displaying the logic devices and the guard ring symbolically and schematically in a single integrated display. Claim 25 defines this feature as follows: "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display." This feature is described at various points in the specification, for example paragraph [0056] describes this feature as follows: "the guard ring P-cell 131 and hierarchical ESD P-cell 132 are combined to form the ESD guard ring hierarchical design 130". This is shown in Figure 13.

Another feature of the invention is the displaying of the logic devices and the guard ring symbolically comprises displaying a parameterized symbol. Claim 25 defines this feature as follows: "wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol." This feature is described at various points in the specification, for example paragraph [0043] describes this feature as follows: "a design system structure of the present invention that integrates a

parameterized cell (P-cell) design 10 and definition 13 using graphical 11 and schematic 12 representations ". This is shown in Figure 1.

Another feature of the invention is the parameterized symbol comprises parameters. Claim 25 defines this feature as follows: "wherein said parameterized symbol comprises parameters." This feature is described at various points in the specification, for example paragraph [0053] describes this feature as follows: "parameterized cell contains both graphical and circuit representation, as well as a symbol function". This is shown in Figure 10.

Another feature of the invention is the parameters comprise at least one of a type of the guard ring and an efficiency of the guard ring. Claim 25 defines this feature as follows: "wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring." This feature is described at various points in the specification, for example paragraph [0053] describes this feature as follows: "By integrating a guard ring P-cell 100 with the ESD P-cell, parasitic devices, the guard ring efficiency, and latchup robustness can be evaluated". This is shown in Figure 10.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44 are anticipated under 35 U.S.C. §102(b) by Ker.

VII. ARGUMENT

A. The Rejection Based on Ker

1. The Position in the Office Action

The Office Action states:

With respect to claims 1, 13, and 25, Ker discloses a computer storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of displaying a guard ring within (hierarchical) (the double guard rings are often used to surround the output PMOS and NMOS in I/O cells ... the additional guard rings should be placed between the I/O cells and the Internal circuits.) (Page 113, cot 2, paragraph 3 and figures 3 and 4(b)) an integrated circuit design having logic devices ("Guard Ring Automation" program to realize the additional guard rings in the layout is proposed to make the layout more automatically and accurately) (The Abstract, page 113), said method comprising:

determining positions of said logic devices within (claim 13, a portion of said hierarchical) said integrated circuit design (the location to be added the additional guard rings (figure 5, Page 115, col. 1, paragraph 2; the signal lines such as a, b, c, d, e, and f pass through the region where to be added the guard ring (figure 5, page 115, paragraphs I and 2); and the double guard rings are often used to surround the output PMOS and NMOS in I/O cells ... the additional guard rings should be placed between the I/O cells and the Internal circuits.) (page 113, col. 2, paragraph 3);

incorporating (forming/adding) said guard ring into (claim 13, said portion of said hierarchical) said integrated circuit design (automatically place the guard ring in the chip

layout to improve latchup immunity of the CMOS IC's (the Abstract); Guard rings are formed by the p+ diffusions in the p-substrate connect to VSS and the n~ diffusions in the n-well connect to VOD. To effectively absorb the trigger current in the well or substrate, the contacts for connection to guard rings should be added as many as possible, (Page 114, Section 2. Guard Rings Automation) and figures 5 and 6 show the guard rings before and after added); and

displaying (claim 13, said portion of) said logic devices and guard ring symbolically (figs 3 through fig. 8) and schematically (circuit) (figs 3 through fig. 8) in a single integrated display (the instance show in Fig. 4(a) and 4(b) are displayed in the master layout views. To simplify the display in the top-level design.. ..)(page 114, section 2.1 Instance and Mosaic, figure 4 descriptions), wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol (figure 4 and its description as page 114-115) wherein said parameterized symbol comprises parameters (10 guard ring, Additional guard ring, p+ diffusion, n+ diffusion, Power line, signal lines... etc)(figs. 1-6,with the description) wherein said parameters comprise at least one of a type of said guard ring (n-type and p-type of guard rings) (figure 4 and its description as page 114-115) and an efficiency of said guard ring (the program will use instance to get the most area efficiency in the guard ring placement. Thus, the proposed Guard Ring Automation program gets a balance between the speed and the are efficiency to add the additional guard rings for latchup prevention) (type of guard rings such as p-diffusion ring and n-diffusion ring; dimension of guard ring such as D horizontal= the width of guard ring region, D vertical= the height of guard ring region;

placement depending on the shape of guard ring such as non-rectangle shape use the instance to add the guard ring and rectangle shape use mosaic to add the guard ring; the electrical connection of guard ring such as p+ diffusions in the p-substrate connect to VSS and the n+ diffusions in the n-well connect to VDD) (pages 114-115 and figures 3-6 and 8.

With respect to claims 30 and 39, Ker discloses all the limitations in set forth claims, further comprising displaying said logic devices and said guard ring graphically in said single display (pages 114-116 and figures 3-6 and 8).

With respect to claims 5, 17, and 29, Ker discloses all the limitations in set forth claims wherein said displaying of said logic devices displays and said guard ring graphically comprise illustrating relative position of said logic device and guard ring (W instance and H instance; D horizontal and D vertical) (figures 4 and 5 and their descriptions; and pages 114-115).

With respect to claims 33, 35-36, 38, 42, and 44, Ker discloses all the limitations in set forth claims, wherein said displaying of said parameterized symbol comprises displaying said parameters including (as per claims 33, 35-36, 38, 42, and 44) a type of circuit (p-substrate/n-well, I/O circuit and internal circuit) and (as per claims 35, 38, and 44) an efficiency of said guard ring (the program will use instance to get the most area efficiency in the guard ring placement. Thus, the proposed Guard Ring Automation program gets a balance between the speed and the are efficiency to add the additional guard rings for latchup prevention) (type of guard rings such as p-diffusion ring and n-diffusion ring; dimension of guard ring such as D horizontal= the width of guard ring

region, D vertical= the height of guard ring region; placement depending on the shape of guard ring such as non-rectangle shape use the instance to add the guard ring and rectangle shape use mosaic to add the guard ring; the electrical connection of guard ring such as p+ diffusions in the p-substrate connect to VSS and the n+ diffusions in the n-well connect to VDD) (pages 114-115 and figures 3-6 and 8).

2. Appellants' Position

a. Independent Claim 1

Appellants traverse the rejections because Ker fails to disclose the claimed features of "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display". Such features are defined in independent claim 1 using identical language.

More specifically, as shown in FIG. 14 of Appellants' disclosure, item 141 illustrates logic devices displayed schematically; item 142 illustrates a guard ring displayed symbolically; and, item 140 illustrates a combination of item 141 and 142; i.e., the logic devices and guard ring are displayed symbolically and schematically in a single integrated display.

To the contrary, Ker does not provide a single integrated display that has *both* symbolic and schematic representations of a guard ring and logic devices. Instead, Ker merely displays "layout views" of component "shapes", wherein the layout views lack schematics. As more fully discussed below, referencing FIG. 4 of Ker, the Office Action argues that the "layout of circuit design … must be constructed from a schematic".

However, Appellants submit that such a schematic is not *displayed in combination* with the layout view "in a single integrated display". As further discussed below, although the Office Action argues that FIGS. 1-3 of Ker display schematics, FIGS. 1-3 do not provide a *single* integrated display that has *both* schematic *and symbolic* representations of a guard ring and logic devices as required by Appellants' claims.

In other words, nothing within Ker discloses a schematic representation of a guard ring and logic devices, and a symbolic representation of the guard ring and logic devices, wherein the schematic representation and the symbolic representation are displayed in a single integrated display. Instead, Ker teaches separately displaying views of the guard ring and logic devices in multiple displays. To the contrary, as illustrated in FIG. 14 of Appellants' disclosure, item 140 illustrates logic devices displayed schematically (item 141) in combination with a guard ring displayed symbolically (item 142).

The Office Action argues that FIGS. 4(a) and 4(b) of Ker disclose displaying logic devices and a guard ring symbolically and schematically in a single display (Office Action, p. 3, item. 5). Appellants respectfully traverse this rejection and submit that FIGS. 4(a) and 4(b) of Ker do not disclose displaying logic devices and a guard ring *schematically*. FIGS. 4(a) and 4(b) of Ker do not illustrate the functional device components schematically; instead, "layout views" showing component "shapes" are displayed *without schematics*.

Specifically, as provided in page 114, column 1, section 2.1 of Ker, to provide the connection from the power lines to the guard rings, a cell called as "instance" was setup

in a cell library. The "shapes of such instances in different CMOS processes are shown in Fig. 4(a) and 4(b)". Further, the Figure description on page 114, column 2, describes "Layout of the instances". However, FIGS. 4(a) and 4(b) do not display the instances symbolically *and schematically*. FIGS. 4(a) and 4(b) lack a schematic representation of the guard ring and a schematic representation of the logic devices. The Office Action argues that the instances of FIGS. 4(a) and 4(b) "must be constructed from a schematic" (Office Action, p. 7, para. 1). However, such a schematic is not displayed in FIGS. 4(a) and 4(b) in combination with a symbolic representation of the guard ring and logic devices in a single integrated display. Appellants further note that the circuit illustrated in Fig. 1(b) is not displayed to the user in a display component.

Further, the circuit illustrated in FIG. 1(b) of Ker does not display a symbolic representation of a guard ring and logic devices. As such, FIG. 1(b) of Ker does not disclose "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" (independent claim 1). Moreover, FIGS. 4(a) and 4(b) of Ker does not display a schematic representation of a guard ring and logic devices. As such, 4(a) and 4(b) of Ker do not disclose "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" (independent claim 1).

In addition, the Office Action argues that schematics are shown in FIGS. 1-3 of Ker (Office Action, p. 7, para. 1). The fact that multiple figures are referenced supports Appellants' position that logic devices and the guard ring are not displayed in a *single integrated* display. Specifically, the Office Action must reference three *different* figures

to illustrate schematic displays and symbolic displays. The Office Action is unable to point to a *single* figure that has *both* schematic *and* symbolic representations of the guard ring and logic devices displayed in a *single integrated* display. To the contrary, as claimed and illustrated in FIG. 14 of Appellants' disclosure, item 140 displays logic devices and a guard ring *both* symbolically *and* schematically in a *single integrated* display.

Accordingly, Appellants submit that unlike the claimed invention, Ker does not disclose displaying logic devices and the guard ring symbolically and schematically in a single display. Instead, "layout views" showing component "shapes" are displayed in Ker without schematics. Therefore, it is Appellants' position that Ker does not disclose the claimed features of "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" as defined in independent claim 1. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

b. Independent Claim 13

Appellants traverse the rejections because Ker fails to disclose the claimed features of "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display". Such features are defined in independent claim 13 using identical language.

More specifically, as shown in FIG. 14 of Appellants' disclosure, item 141 illustrates logic devices displayed schematically; item 142 illustrates a guard ring

displayed symbolically; and, item 140 illustrates a combination of item 141 and 142; i.e., the logic devices and guard ring are displayed symbolically and schematically in a single integrated display.

To the contrary, Ker does not provide a single integrated display that has *both* symbolic and schematic representations of a guard ring and logic devices. Instead, Ker merely displays "layout views" of component "shapes", wherein the layout views lack schematics. As more fully discussed below, referencing FIG. 4 of Ker, the Office Action argues that the "layout of circuit design … must be constructed from a schematic". However, Appellants submit that such a schematic is not *displayed in combination* with the layout view "in a single integrated display". As further discussed below, although the Office Action argues that FIGS. 1-3 of Ker display schematics, FIGS. 1-3 do not provide a *single* integrated display that has *both* schematic *and symbolic* representations of a guard ring and logic devices as required by Appellants' claims.

In other words, nothing within Ker discloses a schematic representation of a guard ring and logic devices, and a symbolic representation of the guard ring and logic devices, wherein the schematic representation and the symbolic representation are displayed in a single integrated display. Instead, Ker teaches separately displaying views of the guard ring and logic devices in multiple displays. To the contrary, as illustrated in FIG. 14 of Appellants' disclosure, item 140 illustrates logic devices displayed schematically (item 141) in combination with a guard ring displayed symbolically (item 142).

The Office Action argues that FIGS. 4(a) and 4(b) of Ker disclose displaying logic devices and a guard ring symbolically and schematically in a single display (Office

Action, p. 3, item. 5). Appellants respectfully traverse this rejection and submit that FIGS. 4(a) and 4(b) of Ker do not disclose displaying logic devices and a guard ring *schematically*. FIGS. 4(a) and 4(b) of Ker do not illustrate the functional device components schematically; instead, "layout views" showing component "shapes" are displayed *without schematics*.

Specifically, as provided in page 114, column 1, section 2.1 of Ker, to provide the connection from the power lines to the guard rings, a cell called as "instance" was setup in a cell library. The "shapes of such instances in different CMOS processes are shown in Fig. 4(a) and 4(b)". Further, the Figure description on page 114, column 2, describes "Layout of the instances". However, FIGS. 4(a) and 4(b) do not display the instances symbolically *and schematically*. FIGS. 4(a) and 4(b) lack a schematic representation of the guard ring and a schematic representation of the logic devices. The Office Action argues that the instances of FIGS. 4(a) and 4(b) "must be constructed from a schematic" (Office Action, p. 7, para. 1). However, such a schematic is not displayed in FIGS. 4(a) and 4(b) in combination with a symbolic representation of the guard ring and logic devices in a single integrated display. Appellants further note that the circuit illustrated in Fig. 1(b) is not displayed to the user in a display component.

Further, the circuit illustrated in FIG. 1(b) of Ker does not display a symbolic representation of a guard ring and logic devices. As such, FIG. 1(b) of Ker does not disclose "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" (independent claim 13). Moreover, FIGS. 4(a) and 4(b) of Ker does not display a schematic representation of a guard ring and logic

devices. As such, 4(a) and 4(b) of Ker do not disclose "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" (independent claim 13).

In addition, the Office Action argues that schematics are shown in FIGS. 1-3 of Ker (Office Action, p. 7, para. 1). The fact that multiple figures are referenced supports Appellants' position that logic devices and the guard ring are not displayed in a *single integrated* display. Specifically, the Office Action must reference three *different* figures to illustrate schematic displays and symbolic displays. The Office Action is unable to point to a *single* figure that has *both* schematic *and* symbolic representations of the guard ring and logic devices displayed in a *single integrated* display. To the contrary, as claimed and illustrated in FIG. 14 of Appellants' disclosure, item 140 displays logic devices and a guard ring *both* symbolically *and* schematically in a *single integrated* display.

Accordingly, Appellants submit that unlike the claimed invention, Ker does not disclose displaying logic devices and the guard ring symbolically and schematically in a single display. Instead, "layout views" showing component "shapes" are displayed in Ker without schematics. Therefore, it is Appellants' position that Ker does not disclose the claimed features of "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" as defined in independent claim 13. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

In addition, Appellants traverse the rejections because Ker fails to disclose the claimed features of "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display". Such features are defined in independent claim 13 using identical language.

More specifically, as discussed in paragraph 0048 of Appellants' disclosure, FIG. 5 is a flowchart that illustrates that the invention first identifies the type of circuit (and the type of ESD protection) 50. This allows the invention to create a parameterized cell (P-cell) 51. The invention then selects the appropriate type of guard ring and places the guard ring within the P-cell 52. *The combined guard ring and P-cell are produced and can be used in a hierarchical circuit design 53.* As further discussed in paragraph 0056 of Appellants' disclosure, FIG. 13 illustrates a hierarchical structure used for the graphical, circuit schematic, or symbol hierarchy. In FIG. 13, *the guard ring P-cell 131 and hierarchical ESD P-cell 132 are combined to form the ESD guard ring hierarchical design 130.*

Moreover, as discussed in paragraph 0051 of Appellants' disclosure, FIG. 7 is a graphical illustration of an input node ESD P-cell that can be used in a hierarchical design. This *parameterized cell* includes voltage lines VDD 70 and VSS 72 P+/N- well diodes 71 that are positioned between the stretch lines 73. This parameterized cell can be auto-generated and actually contains two primitive parameterized (twin diodes). FIG. 8 illustrates the same structure as that shown in FIG. 7 and includes the *guard ring 80.* In this implementation, the new parameterized cell is modified in that it is now contain all

the data information of the parameterized cell guard as well as the ESD parameterized cell.

To the contrary, nothing within Ker discloses the claimed (claim 13) hierarchical integrated circuit design having a parameterized cell and a guard ring. Instead, Ker merely discloses an integrated circuit design having guard rings. Although the Office Action argues that Ker teaches the use of double guard rings (Office Action, p. 4, item 6), nothing within Ker discloses a hierarchical integrated circuit design including such guard rings and a parameterized cell.

In support of its arguments, the Office Action references FIGS. 4(a) and 4(b) of Ker, wherein the Office Action asserts that Ker discloses multiple guard rings. However, the "layout of the instances" shown in FIGS. 4(a) and 4(b) of Ker does not include a hierarchical integrated circuit design. Moreover, the "layout of the instances" shown in FIGS. 4(a) and 4(b) of Ker does not include a parameterized cell. Therefore, it is Appellants' position that Ker fails to disclose the claimed features of "displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and said at least one guard ring" as defined by independent claim 13. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

c. Independent Claim 25

Appellants traverse the rejections because Ker fails to disclose the claimed features of "displaying said logic devices and said guard ring symbolically and

schematically in a single integrated display". Such features are defined in independent claim 25 using identical language.

More specifically, as shown in FIG. 14 of Appellants' disclosure, item 141 illustrates logic devices displayed schematically; item 142 illustrates a guard ring displayed symbolically; and, item 140 illustrates a combination of item 141 and 142; i.e., the logic devices and guard ring are displayed symbolically and schematically in a single integrated display.

To the contrary, Ker does not provide a single integrated display that has *both* symbolic and schematic representations of a guard ring and logic devices. Instead, Ker merely displays "layout views" of component "shapes", wherein the layout views lack schematics. As more fully discussed below, referencing FIG. 4 of Ker, the Office Action argues that the "layout of circuit design … must be constructed from a schematic". However, Appellants submit that such a schematic is not *displayed in combination* with the layout view "in a single integrated display". As further discussed below, although the Office Action argues that FIGS. 1-3 of Ker display schematics, FIGS. 1-3 do not provide a *single* integrated display that has *both* schematic *and symbolic* representations of a guard ring and logic devices as required by Appellants' claims.

In other words, nothing within Ker discloses a schematic representation of a guard ring and logic devices, and a symbolic representation of the guard ring and logic devices, wherein the schematic representation and the symbolic representation are displayed in a single integrated display. Instead, Ker teaches separately displaying views of the guard ring and logic devices in multiple displays. To the contrary, as illustrated in FIG. 14 of

Appellants' disclosure, item 140 illustrates logic devices displayed schematically (item 141) in combination with a guard ring displayed symbolically (item 142).

The Office Action argues that FIGS. 4(a) and 4(b) of Ker disclose displaying logic devices and a guard ring symbolically and schematically in a single display (Office Action, p. 3, item. 5). Appellants respectfully traverse this rejection and submit that FIGS. 4(a) and 4(b) of Ker do not disclose displaying logic devices and a guard ring *schematically*. FIGS. 4(a) and 4(b) of Ker do not illustrate the functional device components schematically; instead, "layout views" showing component "shapes" are displayed *without schematics*.

Specifically, as provided in page 114, column 1, section 2.1 of Ker, to provide the connection from the power lines to the guard rings, a cell called as "instance" was setup in a cell library. The "shapes of such instances in different CMOS processes are shown in Fig. 4(a) and 4(b)". Further, the Figure description on page 114, column 2, describes "Layout of the instances". However, FIGS. 4(a) and 4(b) do not display the instances symbolically *and schematically*. FIGS. 4(a) and 4(b) lack a schematic representation of the guard ring and a schematic representation of the logic devices. The Office Action argues that the instances of FIGS. 4(a) and 4(b) "must be constructed from a schematic" (Office Action, p. 7, para. 1). However, such a schematic is not displayed in FIGS. 4(a) and 4(b) in combination with a symbolic representation of the guard ring and logic devices in a single integrated display. Appellants further note that the circuit illustrated in Fig. 1(b) is not displayed to the user in a display component.

Further, the circuit illustrated in FIG. 1(b) of Ker does not display a symbolic representation of a guard ring and logic devices. As such, FIG. 1(b) of Ker does not disclose "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" (independent claim 25). Moreover, FIGS. 4(a) and 4(b) of Ker does not display a schematic representation of a guard ring and logic devices. As such, 4(a) and 4(b) of Ker do not disclose "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" (independent claim 25).

In addition, the Office Action argues that schematics are shown in FIGS. 1-3 of Ker (Office Action, p. 7, para. 1). The fact that multiple figures are referenced supports Appellants' position that logic devices and the guard ring are not displayed in a *single integrated* display. Specifically, the Office Action must reference three *different* figures to illustrate schematic displays and symbolic displays. The Office Action is unable to point to a *single* figure that has *both* schematic *and* symbolic representations of the guard ring and logic devices displayed in a *single integrated* display. To the contrary, as claimed and illustrated in FIG. 14 of Appellants' disclosure, item 140 displays logic devices and a guard ring *both* symbolically *and* schematically in a *single integrated* display.

Accordingly, Appellants submit that unlike the claimed invention, Ker does not disclose displaying logic devices and the guard ring symbolically and schematically in a single display. Instead, "layout views" showing component "shapes" are displayed in Ker without schematics. Therefore, it is Appellants' position that Ker does not disclose

the claimed features of "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" as defined in independent claim 25. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

d. Dependent Claims 5, 17, and 29

It is Appellants' position that Ker does not disclose the features defined in independent claims 1, 13, and 25 and similarly does not disclose the features defined in dependent claims 5, 17, and 29. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

e. Dependent Claims 30 and 39

It is Appellants' position that Ker does not disclose the features defined in independent claims 1 and 25 and similarly does not disclose the features defined in dependent claims 30 and 39. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

f. Dependent Claims 33, 36, and 42

Appellants traverse the rejections because Ker fails to disclose the claimed feature "wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit". Such features are defined in dependent claims 33, 36, and 42 using identical language.

The Office Action asserts that FIG. 4 of Ker illustrates a parameterized symbol, including whether the guard rings are n-type or p-type (Office Action, p. 4, para. 1). Appellants respectfully disagree with such an assertion.

Specifically, nothing within Ker, including the portions cited by the Office Action, mentions displaying a parameterized symbol, wherein parameters include the type of circuit. Instead, Ker merely teaches that the guard rings are formed by the p+ diffusions in the p-substrate and the n+ diffusions in the n-well (Ker, p. 114, para. 2). Ker also discloses that "[i]f the power line is VDD, the inserted diffusion layer is an N+ diffusion … If the power line is VSS, the inserted diffusion layer is a P+ diffusion … The program can choose the diffusion type (N+ or P+) automatically" (Ker, p. 115, para. 2). Nevertheless, Ker does not disclose that the diffusion type is displayed via a parameterized symbol. Further, neither the p-substrate, the n-well, nor the diffusion type is illustrated in FIG. 4 of Ker.

Accordingly, Appellants submit that Ker does not display a parameterized symbol, including the type of circuit. Therefore, it is Appellants' position that Ker fails to disclose the claimed features of "wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit" as defined in dependent claims 33, 36, and 42.

g. Dependent Claims 35, 38, and 44

Appellants traverse the rejections because Ker fails to disclose the claimed feature "wherein said displaying of said parameterized symbol comprises displaying said

parameters including a type of circuit and an efficiency of said guard ring". Such features are defined in dependent claims 33, 36, and 42 using identical language.

The Office Action asserts that FIG. 4 of Ker illustrates a parameterized symbol, including the efficiency of the guard rings (Office Action, p. 4, para. 1). Appellants respectfully disagree with such an assertion.

Specifically, nothing within Ker, including the portions cited by the Office Action, mentions displaying a parameterized symbol, wherein parameters include the efficiency of the guard rings. Instead, Ker merely discloses placing the guard ring to improve "area efficiency". As described on page 115, paragraph 3 of Ker, the program will use instance to get the most area efficiency in the guard ring placement. Thus, the proposed Guard Ring Automation program gets a balance between the speed and the area efficiency to add the additional guard rings for latchup prevention.

Accordingly, Ker discloses an automated program for placing guard rings that improves "area efficiency"; Ker does not display a parameterized symbol, wherein parameters include the efficiency of the guard rings. Therefore, it is Appellants' position that Ker does not disclose the claimed features "wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit and an efficiency of said guard ring" as defined in dependent claims 33, 36, and 42.

B. CONCLUSION

In view the forgoing, the Board is respectfully requested to reconsider and withdraw the rejections of claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Date: July 25, 2007

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IX. CLAIMS APPENDIX

1. A method of displaying a guard ring within an integrated circuit design having logic devices, said method comprising:

determining positions of said logic devices within said integrated circuit design;

incorporating said guard ring into said integrated circuit design; and

displaying said logic devices and said guard ring symbolically and schematically in a single integrated display,

wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol,

wherein said parameterized symbol comprises parameters, wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring.

2-4. (Cancelled).

5. The method in claim 30, wherein said displaying of said logic devices and said guard ring graphically comprises illustrating relative positions of said logic devices and said guard ring.

6-12. (Cancelled).

13. A method of displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and said at least one guard ring, said method comprising:

establishing positions of said logic devices within a portion of said hierarchical integrated circuit design;

incorporating said guard ring into said portion of said hierarchical integrated circuit design; and

displaying said portion of said integrated circuit design as a cell having said guard ring within said hierarchical integrated circuit design,

wherein said displaying of said portion of said integrated circuit design comprises displaying said logic devices and said guard ring symbolically and schematically in a single integrated display,

wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol,

wherein said parameterized symbol comprises parameters, wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring.

14-16. (Cancelled).

17. The method in claim 13, wherein said displaying of said portion of said integrated circuit design comprises graphically illustrating relative positions of said logic devices

and said guard ring.

18-24. (Cancelled).

25. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of displaying a guard ring within an integrated circuit design having logic devices, said method comprising:

determining positions of said logic devices within said integrated circuit design;

incorporating said guard ring into said integrated circuit design; and

displaying said logic devices and said guard ring symbolically and schematically in a single integrated display,

wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol,

wherein said parameterized symbol comprises parameters, wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring.

26-28. (Cancelled).

29. The program storage device in claim 39, wherein said displaying of said logic devices and said guard ring graphically comprises illustrating relative positions of said logic devices and said guard ring.

30. The method in claim 1, further comprising displaying said logic devices and said guard ring graphically in said single display.

31-32. (Cancelled).

33. The method in claim 1, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit.

34. (Cancelled).

35. The method in claim 1, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit and an efficiency of said guard ring.

36. The method in claim 13, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit.

37. (Cancelled).

38. The method in claim 13, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit and an efficiency of said

guard ring.

39. The program storage device in claim 25, further comprising displaying said logic devices and said guard ring graphically in a single display.

40-41. (Cancelled).

42. The program storage device in claim 25, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit.

43. (Cancelled).

44. The program storage device in claim 25, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit and an efficiency of said guard ring.

X. EVIDENCE APPENDIX

There is no other evidence known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There is no other related proceedings known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.